

SN 09/450,054



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:

Appellant(s): **Ashok V. Krishnamoorthy**  
Case: **Krishnamoorthy 32**  
Serial No.: **09/450,054** Filed: **November 22, 1999**  
Examiner: **Cornelius H. Jackson** Group Art Unit: **2828**  
Title: **POWER DISTRIBUTION NETWORK FOR OPTOELECTRONIC  
CIRCUITS**

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BRIEF ON APPEAL

SIR:

The following Appeal Brief is submitted to the Board of Patent Appeals and Interferences on appeal from the decision of the Examiner of Group Art Unit 2828 dated November 19, 2003, finally rejecting claims 1-11 and pursuant to the Notice of Appeal

filed on March 16, 2004 and received by the Patent Office on March 16, 2004 in the above-identified application.

### **REAL PARTY IN INTEREST**

The real party in interest is Lucent Technologies, Inc.

### **RELATED APPEALS AND INTERFERENCES**

No other appeals or interferences that directly affect, or are directly affected by, or have a bearing on the Board's decision in the pending appeal are known to the Appellant, Appellant's legal counsel, or the assignee.

### **STATUS OF THE CLAIMS**

Claims 1-11 stand under final rejection, from which rejection this appeal is taken.

### **STATUS OF AMENDMENTS**

A first response was filed on February 13, 2002 in response to a First Office Action dated December 19, 2001 (Paper No. 3). In the first Office Action, the Examiner noted that claims 1-11 were pending and that claims 1-11 were rejected. In the response, no amendments were made.

A second response was filed on June 19, 2002 in response to a Second Office Action dated April 24, 2002 (Paper No. 6). In the Second Office Action, the Examiner noted that claims 1-11 were pending in the application and that claims 1-11 were rejected. In the response, Claims 2-6, 8 and 9 were amended to correct for informalities pointed out by the Examiner and not in response to prior art.

A third response was filed on November 25, 2002 in response to a Final Office Action dated September 24, 2002 (Paper No. 8) and in response to a telephone interview with the Examiner. In the Final Office Action, the Examiner noted that claims 1-11 were pending in the application and that claims 1-11 were rejected. In the response, Claims 1, 7 and 10 were amended to more clearly define the Appellant's invention as suggested by the Examiner and not in response to prior art.

An Advisory Action dated December 27, 2002 (Paper No. 10) was received by the Appellant indicating that the amendments in the Appellant's response to the Final Office Action would not be entered because the amendments raised new issues that would require further consideration and a new search. A fourth response was filed on January 23, 2003 in response to an Advisory Action dated December 27, 2002 (Paper No. 10) and in response to a telephone interview with the Examiner. In the telephone interview, the Examiner agreed with the Appellant that the Appellant's response to the Final Office Action did not require a new search and as such the Finality of the Office Action was withdrawn. The Appellant's amendments to Claims 1, 7 and 10 in his response to the Final Office Action were entered.

A fifth response was filed on May 20, 2002 in response to an Office Action dated February 27, 2003 (Paper No. 12). In the Office Action, the Examiner noted that claims 1-11 were pending in the application and that claims 1-11 were rejected. In the response, no amendments were made.

A sixth response was filed on September 15, 2003 in response to an Office Action dated June 16, 2003 (Paper No. 14). In the Office Action, the Examiner noted that claims 1-11 were pending in the application and that claims 1-11 were rejected. In the response, Claims 1, 7, 10 and 11 were amended to more clearly define the Appellant's invention and not in response to prior art.

A seventh response was filed on January 15, 2004 in response to a Final Office Action dated November 19, 2003 (Paper No. 16). In the Final Office Action, the Examiner noted that claims 1-11 were pending in the application and that claims 1-11 were rejected. In the response, Claims 1 and 7 were amended to more clearly define the Appellant's invention and not in response to prior art.

An Advisory Action dated February 18, 2004 was received by the Appellant indicating that the amendments in the Appellant's response to the Final Office Action would be entered and stating an explanation of how the new or amended claims would be rejected.

The claims on appeal are those in the Final Office Action response filed January 15, 2004.

### **SUMMARY OF THE INVENTION**

The present invention provides a solution to the problem of maintaining a constant bias voltage associated with distributing a power signal to optoelectronic devices in an optoelectronic circuit. The power distribution network of the present invention includes electrically conductive pathways that form at least one level, where each level includes a plurality of equal-length conductive segments, a means for coupling the power signal from a primary input to a point at the center of a first level, terminal nodes coupled at the extremities of a last level for supplying the power signal to devices that form at least a portion of the optoelectronic circuit, and wherein the number of segments connecting the primary input to each of the terminal nodes is equal. Because the length of each of the conductive pathways from the primary input to each terminal node is equal, greater bias voltage uniformity is provided to the terminal nodes.

For example, in one illustrative embodiment, the power distribution network for optoelectronic circuits includes electrical conductive pathways that form an H-tree network that distributes a power signal to a plurality of terminal nodes, for example, VCSELs on an optoelectronic chip. The H-tree network includes a primary input for receiving a power signal and a plurality of equal length conductive pathways that are arranged to form a plurality of levels, wherein portions of said conductive pathways are interconnected. Each level has a plurality of equal length segments (branches) that forms at least one Arabic letter "H"-shaped patterns. Each H pattern includes six equal length segments, with two segments in each of two parallel portions and two segments connected perpendicular at the midpoints of the parallel portions to form the H pattern. The pluralities of segments are laid out in a hierarchical succession of H patterns to form the various levels of the H-tree network. The first level is coupled to the primary input, at the midpoint of the two perpendicular segments of the H pattern. A new level of the H-tree is formed by coupling the center of the two perpendicular segments of the new level H patterns to the end points of the preceding level H patterns of the H-tree. Terminal nodes are coupled to the end points of the last level of the H-tree. In this manner a conductive pathway is formed from the primary input to each terminal node, with portions of each conductive pathway interconnected with one or more other

conductive pathways. Since the length of each segment is equal, the length of the conductive pathway from the primary input to each terminal node is the same. In operation, the power distribution tree network utilizes the equal lengths of the conductive pathways of the H-tree network to provide greater bias voltage uniformity to the terminal nodes by eliminating small differences in bias voltage to terminal nodes in different locations of the optoelectronic circuit.

In another illustrative embodiment, the power distribution network includes an H-tree network, which is configured in an H-tree geometrical pattern that ensures that the absolute voltage at each terminal node is not affected by current consumption of other terminal nodes in the optoelectronic circuit. The H-tree geometrical pattern is similar to the embodiment described above except that each terminal node has a separate conductive pathway associated with it. Specifically, the conductive pathways from the primary input to each terminal node are not shared for any portion of the pathway. Each conductive pathway is equal in length but is joined to other conductive pathways only at a common point.

For the convenience of the Board of Patent Appeals and Interferences, Appellant's claim 1 (one of the broadest independent claims) is presented below in claim format as suggested in MPEP 1206. Claim 1 positively recites:

A network for distributing a power signal in an optoelectronic circuit, said network comprising:

a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths, and wherein the segments of a next order higher level are formed at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point for the formation of the next order higher level;

means for coupling said power signal from a primary input to the common point of the first level; and

terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal.

### **ISSUES**

1. Whether claims 1-2, 4-5 and 10-11 are Patentable under 35 U.S.C. §102(b) over Koh et al. U.S. Patent No. 5,416,861 (hereinafter "Koh").
2. Whether claims 3 and 6-9 are Patentable under 35 U.S.C. §103(a) over Koh in view of Watanabe U.S. Patent No. 6,309,001.
3. Whether claims 1-5 and 10-11 are Patentable under 35 U.S.C. §103(a) over Watanabe.
4. Whether claims 6-9 are Patentable under 35 U.S.C. §103(a) over Watanabe in view of Olbright et al. U.S. Patent No. 5,266,794 (hereinafter "Olbright")/ Schneider et al. U.S. Patent No. 5,351,256 (hereinafter "Schneider")/ Lebby et al. U.S. Patent No. 5,337,397 (hereinafter "Lebby").

### **Grouping of Claims**

Pending claims 1-2, 4-5, and 10-11; 3 and 6-9; and 1-5 and 10-11 have been grouped together by the Examiner in their rejection. Appellant urges that each of the rejected claims stands on its own recitation, the claims being considered to be separately patentable for the reasons set forth in more detail *infra*.

### **REFERENCES**

The following references are relied on by the Examiner:

- 1) U.S. Patent No. 5,416,861, issued to Koh et al., May 16, 1995.
- 2) U.S. Patent No. 6,309,001, issued to Watanabe, May 3, 1994.
- 3) U.S. Patent No. 5,266,794, issued to Olbright et al., November 30, 1993.
- 4) U.S. Patent No. 5,351,256, issued to Schneider et al., September 27, 1994.
- 5) U.S. Patent No. 5,337,397, issued to Lebby et al., August 9, 1994.

### **Brief Description of the References**

1) In Koh, an optical waveguide H-tree design is provided for global clock distribution on multichip modules (MCM) which has nearly zero clock skew and may be used for a distributed computer system environment. The optical waveguide H-tree design of Koh utilizes channel waveguides, curved sections and directional couplers formed using silica glass and silicon oxynitride (SiON) channel waveguide technologies. In the invention of Koh, the achievable clock speed is limited by a laser diode source and photodiode receiver at each chip module, and not by the optical waveguide distribution network. The high-speed optical waveguide can be configured to transmit clock signals, or for use as a multi-wavelength communication network that communicates signals to various integrated circuits (ICs) mounted on the multichip module. This is achieved using multiple laser diodes having different output wavelengths and directing their outputs into an optical multiplexer. At the receiving points on the ICs, optical demultiplexers filter the optical signals into individual output signals.

2) In Watanabe, a light-emitting diode having a surface electrode of a tree-like form is disclosed. A surface electrode on a surface of a LED has a pad, and further, first-order branches linearly extending from the pad, second-order branches diverged and linearly extending from the first-order branches, and third-order branches diverged and linearly extending from the second-order branches. The pad out of the surface electrode is not in electrical contact with a underlying semiconductor layer, whereas the surface electrode and the semiconductor layer are in electrical contact with each other at ends of the highest-order branches. Also, the semiconductor layer is provided along a pattern of the surface electrode in a mesa shape. As such, Watanabe alleges that ineffective light emission underneath the surface electrode is relatively reduced so that external quantum efficiency can be improved, and moreover even shorter-wavelength light can be allowed to go out at high efficiency by omitting a current diffusion layer.

3) In Olbright, a method for vertical-cavity surface emitting laser optical interconnection is disclosed having a stack of vertically aligned optoelectronic integrated (OEIC)

modules. Each OEIC module includes an array of vertical cavity surface emitting lasers (VCSEL), receivers and electronic logic which are monolithically integrated on a single semiconductor substrate. Communication between the OEIC modules is effectuated by the free space propagation of laser radiation from the VCSELs to corresponding receivers on an adjacent OEIC module. Transistors, such as heterojunction bipolar transistors, may be used to drive the VCSELS.

4) In Schneider, an electrically injected visible vertical cavity surface emitting laser diode is disclosed. Visible laser light output from an electrically injected vertical cavity surface emitting laser (VCSEL) diode is enabled by the addition of phase-matching spacer layers on either side of the active region to form the optical cavity. The spacer layers comprise InAlP which act as charge carrier confinement means. Distributed Bragg reflector layers are formed on either side of the optical cavity to act as mirrors. Schneider alleges that the electrically injected VCSEL diode of the invention is operable chiefly because of a new cavity design. The structure starts with conventional elements of an InGaP/InAlGaP strained quantum well active cavity and AlAs/Al.sub.0.5Ga.sub.0.5As DBR's. The advance is in the addition of relatively thick InAlP optical phase-matching spacer layers on either side of the SQW region to fill out the remainder of the multiple  $\lambda/2$  thickness of the Fabry-Perot cavity. Schneider alleges that this and several other improvements result in the first VCSEL diode able to emit in the visible spectrum.

5) In Lebby, a method is provided for coupling a light emitting device to a core region of an optical waveguide. An optical waveguide having a core region with an end and a cladding region is formed. The cladding region surrounds the end of the core region, as well as forming a surface having a lens device thereon. The end of the core region is positioned to provide a selected distance from the lens device to the end of the core region of the waveguide. A light emitting device having a working portion is mounted on the surface of the cladding region with the working portion of the light emitting device directed over the lens device for collection and focusing of light from the working portion of the light emitting device into the end of the core region. Lebby alleges that an

advantage of the present invention is to relax alignment tolerances between the working portion of the light emitting device and the core region of the waveguide and to provide a more manufacturable process.

### **ARGUMENT**

#### **The Issues Under 35 U.S.C. §102**

- I. **THE EXAMINER ERRED IN REJECTING CLAIMS 1-2, 4-5 AND 10-11 UNDER 35 U.S.C. § 102(b) BECAUSE THE CITED REFERENCE FAILS TO TEACH, SHOW, OR SUGGEST AT LEAST A PLURALITY OF ELECTRICALLY CONDUCTIVE PATHWAYS FORMING AT LEAST A FIRST LEVEL WHEREIN EACH LEVEL IS COMPRISED OF PLURALITY OF SEGMENTS LINEARLY EXTENDING FROM A COMMON POINT, EACH OF THE SEGMENTS OF RESPECTIVE LEVELS HAVING EQUAL LENGTHS, AND TERMINAL NODES COUPLED AT THE EXTREMITIES OF A LAST LEVEL FOR SUPPLYING A POWER SIGNAL TO A PLURALITY OF DEVICES SUCH THAT THE POWER SUPPLIED BY THE TERMINAL NODES TO EACH OF THE PLURALITY OF DEVICES IS SUBSTANTIALLY EQUAL.**

Claims 1-2, 4-5 and 10-11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Koh on grounds that the reference anticipates each feature of the claimed invention. The rejection is respectfully traversed.

“Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim” (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1983)). (emphasis added).

The Appellant respectfully submits that Koh does not teach, suggest or disclose each and every element of the Appellant’s claimed invention arranged as in the claims. More specifically, Koh discloses an optical waveguide H-tree design for **global clock distribution** on multichip modules (MCM). (See Koh, ABSTRACT). The Appellant respectfully submits that the teachings of Koh do not anticipate the invention of the Appellant. Specifically the Appellant submits that the Examiner has erroneously interpreted the teachings of Koh as teaching a power distribution network including “a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point,

each of the segments of respective levels having equal lengths” and “terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal” as taught and claimed by the Appellant.

The Appellant claims in at least claim 1 “a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths.” As claimed in the Appellant's invention, each of the segments of respective levels of a power distribution network in accordance with the present invention are of equal length such that a power signal input to a power distribution network of the present invention is substantially equally supplied to optoelectronic circuits being supplied the power via terminal nodes at the extremities of a last level. In support of the invention, the Appellant, in the specification specifically discloses:

“A new level of the H-tree is formed by coupling the center of the two perpendicular segments of the new level H patterns to the end points of the preceding level H patterns of the H-tree. In this manner a conductive pathway is formed from the primary input to each terminal node, with portions of each conductive pathway interconnected with one or more other conductive pathways. Since the length of each segment is equal for a respective level, the length of the conductive pathway from the primary input to each terminal node is the same.

In operation, the power distribution tree network utilizes the equal lengths of the conductive pathways of the H-tree network to provide greater bias voltage uniformity to the terminal nodes by eliminating small differences in bias voltage to terminal nodes in different locations of the optoelectronic circuit.” (See Specification, page 3, lines 11-23).

The Appellant, in the Specification, specifically discloses and teaches a power distribution network wherein each of the segments of each level are equal in length. It is evident from at least the portion of the Appellant's disclosure presented above, that the Appellant's invention is directed, at least in part, to a network for distributing a power signal in an optoelectronic circuit wherein **each** of the plurality of segments in each level is of equal length such that a bias voltage for devices connected to the

extremities of a final level experience the same bias voltage. For the distribution of a power signal, unlike for the distribution of a clock signal, it is very important that the segments of each level be equal such that the distribution of the power signal from segment to segment, and from level to level and eventually from the input of the power distribution network to each of the terminal node outputs of the power distribution network is divided evenly such that a bias voltage for devices connected to the extremities of a final level experience the same bias voltage. For the distribution of a clock signal, however, (such as in the clock distribution network taught in Koh) only an entire path length has to be equal. What is important in a clock distribution network (such as in the clock distribution network taught in Koh) is the time that is required for the clock signal to travel from an input to an output.

More specifically and in contrast to the Appellant's invention, there is absolutely no teaching, suggestion or disclosure in Koh for a network for distributing a power signal in an optoelectronic circuit wherein **each** of the plurality of segments in each level is of equal length. The invention of Koh instead is directed to a network for distributing an optical clock signal and not to a network for distributing a power signal in an optoelectronic circuit where **each** of the plurality of segments in each level is of equal length. As described above, what is important, and more specifically, what is taught in Koh, is that a path length from input to output must be equal. In support of this concept, Koh specifically recites:

"While it is preferred to use an completely symmetrical H-tree in constructing the waveguide segments 24 upon MCM 20, that can only occur where each of the ICs 26 has its optical input at a location that allows such ICs 26 to be oriented in a periodic array. In such a circumstance, each of the optical paths within optical clock network 10 can truly be of equal length." (See Koh, col. 18, lines 28-34).

Koh specifically teaches that in such a symmetrical H-tree configuration, what is important is that the path lengths (from input to output) are of equal length. There is absolutely no teaching, suggestion or disclosure in Koh for "a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of

respective levels having equal lengths” as taught by the Appellant’s specification and claimed in at least the Appellant’s claim 1. Again, Koh stresses the importance of having equal total path lengths for a symmetrical clock distribution network, but in no way teaches that each of the plurality of segments in respective levels are of equal length as is required for a power distribution network as taught and claimed by the Appellant. In Koh the segments on one side of a level of a symmetrical clock distribution network may be of unequal length as long as the respective segments on the other side (symmetrical portion) of the clock distribution network of Koh also have similar varying lengths. That is, a symmetrical H-tree configuration for distributing a clock signal as taught in Koh may comprise segments of varying lengths in a single level as long as each of the input to output paths comprise equal lengths.

As such, the Appellant respectfully submits that the Appellant’s invention does have a structural difference over the invention of Koh. Specifically, in the invention of the Appellant, a network for distributing a power signal comprises “a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths”. Koh does not teach, suggest or disclose that each of a plurality of segments making up respective levels all have equal lengths.

In addition, there is absolutely no disclosure in Koh for a “network for distributing a power signal in an optoelectronic circuit, said network comprising a plurality of electrically conductive pathways.” The “segments 24” cited by the Examiner are not “electrically conductive” as claimed. The Koh reference is simply directed to a different problem than the claimed invention, and the problem is solved in a different manner than claimed here. In contrast to the above quoted claim language, Koh discloses an H-tree configuration for clock distribution (i.e., not power distribution) on MCM substrates using optical rather than electrical interconnection. (See Koh, column 10, lines 57-61.) (emphasis added). The power distribution claimed and taught by the Appellant is directed to providing a substantially similar biasing voltage to optoelectronic circuits connected the extremities of a last level of a power distribution network in accordance with the Appellant’s invention. However, there is absolutely no

teaching, suggestion or disclosure in Koh for the equal distribution of a bias voltage via a plurality of equal length segments.

For at least the reasons stated above, the Appellant respectfully submits that the teachings of Koh do not anticipate the invention of the Appellant. Specifically and regarding the Appellant's claim 1, Koh does not teach, suggest or describe a power distribution network having "a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths" and "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal" as taught by the Appellant's Specification and claimed by at least the Appellant's claim 1.

Regarding claim 2, the Appellant further submits that Koh also fails to teach, suggest or disclose a power distribution network having "a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths" and "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal" wherein each level is at least one H-shaped pattern. In claim 2, each H-shaped level comprises first and second parallel branches, each having a respective first and second midpoint, and a third branch interconnecting said first and second midpoints, and wherein the center of the H-shaped pattern is the midpoint of the third branch. As claimed by claim 2, the power distribution network of the present invention must have equal length segments in each respective level.

Regarding claims 4 and 5, the Appellant further submits that Koh also fails to teach, suggest or disclose a power distribution network having "a plurality of electrically

conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths” and “terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal” wherein the network is located on an optoelectronic chip as claimed in claim 4 or wherein the terminal nodes are optoelectronic devices as claimed in claim 5.

Regarding claim 10, the Appellant further submits that Koh also fails to teach, suggest or disclose a method of distributing a power signal to a plurality of terminal nodes on an optoelectronic circuit, wherein a power signal is directed to the plurality of terminal nodes using an H-tree network, the H-tree network including at least a first level, wherein the first level is coupled to said primary input, and a last level includes the plurality of terminal nodes for supplying said power signal to a plurality of devices, each of the at least one level having a plurality of segments, each segment of a respective plurality is equal in length and wherein a number of segments from the primary input to each of the terminal nodes is equal such that the power supplied by each of the terminal nodes to each of the plurality of devices is substantially equal. Koh fails to teach, suggest or disclose the Appellant’s invention of claim 10 for at least the reasons stated above with respect to claim 1.

Regarding claim 11, the Appellant submits that Koh fails to teach, suggest or disclose a method of distributing a power signal to a plurality of terminal nodes on an optoelectronic circuit, wherein a power signal is directed to the plurality of terminal nodes using an H-tree network, said H-tree network including at least a first level, wherein the first level is coupled to said primary input, and a last level includes said plurality of terminal nodes for supplying said power signal to a plurality of devices, each of said at least one level having a plurality of segments, each segment of a respective plurality is equal in length and wherein a number of segments from said primary input to each of said terminal nodes is equal such that the power supplied by each of the terminal nodes to each of the plurality of devices is substantially equal wherein the

directing step further includes directing the power signal to the plurality of terminal nodes using an H-tree network, wherein the plurality of segments are configured into at least one H pattern to form the at least first level, and wherein the at least first level is configured into a hierarchical succession of H patterns as claimed in claim 11.

Therefore, the Appellant submits that claims 1, 2-5 and 10-11 are not anticipated by the teachings of Koh for at least the reasons set forth above and, as such, fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder. Reversal of the rejection is respectfully requested.

### **The Issues Under 35 U.S.C. §103**

**II. THE EXAMINER ERRED IN REJECTING CLAIMS 3 AND 6-9 UNDER 35 U.S.C. § 103(a) BECAUSE THE CITED REFERENCE FAILS TO TEACH, SHOW, OR SUGGEST AT LEAST AT LEAST A PLURALITY OF ELECTRICALLY CONDUCTIVE PATHWAYS FORMING AT LEAST A FIRST LEVEL WHEREIN EACH LEVEL IS COMPRISED OF PLURALITY OF SEGMENTS LINEARLY EXTENDING FROM A COMMON POINT, EACH OF THE SEGMENTS OF RESPECTIVE LEVELS HAVING EQUAL LENGTHS, AND TERMINAL NODES COUPLED AT THE EXTREMITIES OF A LAST LEVEL FOR SUPPLYING A POWER SIGNAL TO A PLURALITY OF DEVICES SUCH THAT THE POWER SUPPLIED BY THE TERMINAL NODES TO EACH OF THE PLURALITY OF DEVICES IS SUBSTANTIALLY EQUAL WHEREIN THE TERMINAL NODES ARE VCSELS, WHEREIN EACH LEVEL IS AT LEAST ONE X-SHAPED PATTERN AND WHEREIN SAID CENTER OF SAID H-SHPED PATTERN IS THE MIDPOINT OF A THIRD BRANCH**

Claims 3 and 6-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Koh in view of Watanabe. The rejection is respectfully traversed.

The Examiner alleges that regarding claim 3, Koh, as applied above to claims 1 and 2, teaches all of the aspects of claim except that the pattern of the level is X-shaped. As such, the Examiner cites Watanabe for teaching that the pattern of the level is X-shaped. The Examiner alleges that regarding claim 6, Koh, as applied above to claims 1 and 2, teaches all of the aspects of claim except that the terminal mode may be a VCSEL but that the use of a VCSEL is merely a design choice. The Appellant respectfully disagrees.

Claims 3 and 6 depend directly from independent claim 1 and recite further limitations thereof. The Examiner applied Koh to claims 3 and 6 as described above for the Examiner's rejection of claim 1. As described above, the teachings of Koh do not teach, suggest or describe the Appellant's invention at least with regard to independent claim 1. Therefore, at least because the teachings of Koh do not teach, suggest, or describe the invention of the Appellant regarding at least claim 1 as discussed herein, the Appellant respectfully submits that the teachings of Koh also do not teach, suggest, or describe the invention of the Appellant regarding dependent claims 3 and 6, which depend from independent claim 1, and, thus do not make obvious the Appellant's claims 3 and 6.

The Appellant further submits that the teachings of Watanabe alone also fail to teach, suggest or describe the invention of the Appellant at least with regard to independent claim 1. That is, the teachings of Watanabe alone, for a light-emitting diode having a surface electrode of a tree-like form (See Watanabe, Abstract), do not make obvious the Appellant's invention at least with regard to independent claim 1. In support of its invention Watanabe teaches:

**"At the ends of the sixth-order branches 358a and 358b, there are provided contact portions 359a and 359b for making ohmic contact with the underlying semiconductor layer 351.** Meanwhile, the rest of the surface electrode 347 other than the contact portions 359a and 359b is in a state in which a Schottky barrier are yielded on the surface of the semiconductor layer 351." (See Watanabe, col. 16, lines 1-7). (emphasis added).

"Further, since the end portions of the sixth-order (highest-order) branches 358a and 358b and the semiconductor layer 351 are put into successful ohmic contact with each other through the contact portions 359a and 359b while the rest other than the end portions and the semiconductor layer 351 are brought into a state in which the current is suppressed from flowing by the Schottky barrier (i.e. a state in which current will not flow unless a certain high level of voltage is applied), the current can be injected only at the end portions of the surface electrode 351. Accordingly, the light easily goes out of the LED, which leads to further improved external quantum efficiency." (See Watanabe, col. 16, lines 38-50).

The structure of the invention of Watanabe, as taught, includes contact portions in the highest-order branches for making ohmic contact with the underlying semiconductor layer. In contrast, the Appellant's invention is directed at least in part to

a power distribution network having very different structural limitations. In support of the present invention, the Appellant discloses:

“Terminal nodes are coupled to the endpoints of the last level of the H-tree. In this manner a conductive pathway is formed from the primary input to each terminal node, with portions of each conductive pathway being shared between two or more terminal nodes.” (See Specification, page 7, lines 13-16).

“The first level is coupled to the primary input, at the center of the two horizontal segments of the H pattern. The conductive pathways distribute a power signal to terminal nodes 16 (represented by circles and as further indicated in the upper right hand quadrant for a portion of the terminal nodes of FIG. 3) on VLSI chip 20, wherein the distance from the primary input to each terminal node 16 is equal. In this illustrative example, **each terminal node 16 represents a VCSEL and its associated driver.**” (See Specification, page 6, lines 22-29). (emphasis added).

“In operation of the present invention, the effect of voltage drops due to power supply line resistance are reduced when DC power is distributed to the terminal nodes of an optoelectronic circuit, namely the VCSELs in an array of VCSELs of an OE-VLSI chip, with the H-tree power distribution network. Since the lengths of the conductive pathways to each terminal node are equal, there is greater uniformity of the voltage and current provided to each terminal node.” (See Specification, page 8, lines 3-8).

It is evident from the Appellant's disclosure, that the Appellant's invention is directed at least in part to a power distribution network for providing uniform power to external devices connected to each terminal node. As such, it is clear that the terminal nodes of the Appellant's invention are not in ohmic contact with an underlying layer. Furthermore, in support of at least claim 1, the Appellant in the Specification specifically recites:

“Each ‘H’ pattern includes six equal length segments, with two segments in each of two parallel portions and two segments connected perpendicular at the midpoints of the parallel portions to form the H pattern.” (See Specification, page 7, lines 3-5).

The Appellant further recites:

“Since the length of each segment is equal for a respective level and the total number of segments to each terminal node is also equal, the length of the conductive pathway from the primary input to each terminal node is the same.” (See Specification, page 7, lines 16-19).

It is apparent from the sections of the disclosure presented above that the Appellant's invention is directed at least in part to a power distribution network wherein each of the segments comprising each layer are of equal lengths and the total number of segments connecting each terminal node the primary input are equal. As such, the power provided to each of the plurality of terminal nodes at a last level and subsequently to each of a plurality of connected devices is substantially equal.

The invention of Watanabe is incapable of providing uniform power to devices connected to each terminal node because the surface electrode and the semiconductor layer are in electrical contact with each other at ends of the highest-order branches. The Appellant respectfully submits that at least the structural differences between the highest-order branches of the Appellant's invention and the highest-order branches of the invention of Watanabe make the Appellant's invention patentable over the invention of Watanabe. The Appellant further submits that the structural configuration of the Appellant's highest-order branches are not obvious in view of the invention of Watanabe. The Appellant's invention and the invention of Watanabe are directed to two different devices having different structural limitations used for solving different problems. There is absolutely no teaching or suggestion in Watanabe for the Appellant's invention at least with respect to claim 1 and specifically for the structural limitations of the terminal nodes of the Appellant's invention as described above. More specifically, there is absolutely no teaching, suggestion or disclosure in Watanabe for "a plurality of electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths" (emphasis added), as taught by the Appellant's specification and claimed in at least the Appellant's claim 1.

Even further, there is absolutely no teaching, suggestion or disclosure in Watanabe for "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal" (emphasis added) as taught by the Appellant's specification and claimed in at least the Appellant's claim 1. Therefore,

the Appellant respectfully submits that the Appellant's invention and the invention of Watanabe are directed to two different devices having different structural limitations used for solving different problems. There is absolutely no teaching or suggestion in Watanabe for the Appellant's invention at least with respect to claim 1 and specifically for the structural limitations of the Appellant's invention as described above.

As such, the Appellant respectfully submits that Watanabe does not teach or suggest the Appellant's claim 1. Specifically, the Appellant submits that the structural limitations of at least the Appellant's claim 1 are not taught or suggested by Watanabe.

The Appellant further submits that there is no suggestion or motivation to combine the teachings of Koh and the teachings of Watanabe.

For prior art reference to be combined to render obvious a subsequent invention under 35 U.S.C. § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. Uniroyal v. Rudkin-Wiley, 5 U.S.P.SQ.2d 1434, 1438 (Fed. Cir. 1988). The teachings of the references can be combined only if there is some suggestion or incentive in the prior art to do so. In re Fine, 5 U.S.P.SQ.2d 1596, 1599 (Fed. Cir. 1988). Hindsight is strictly forbidden. It is impermissible to use the claims as a framework to pick and choose among individual references to recreate the claimed invention Id. at 1600; W.L. Gore Associates, Inc., v. Garlock, Inc., 220 U.S.P.Q. 303, 312 (Fed. Cir. 1983).

Moreover, the mere fact that a prior art structure could be modified to produce the claimed invention would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

The Appellant further submits that even if there was a motivation or suggestion to combine the references (which the Appellant believes that there is none), the teachings of Watanabe fail to bridge the substantial gap between the Appellant's invention, and the teachings of Koh.

As such, and at least for the reason that neither Koh or Watanabe alone or in any combination teach suggest, or describe the Appellant's invention with regard to claim 1, the Appellant respectfully submits that dependent claims 3 and 6, which

depend directly from independent claim 1, are also not rendered obvious by Koh in view of Watanabe.

Therefore, the Appellant submits that dependent claims 3 and 6 as they now stands, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder. Reversal of the rejection is respectfully requested.

Regarding claims 7 and 9, The Examiner applied Koh and Watanabe to claims 7 and 9 as described above for the Examiner's rejection of claims 1 and 3 above.

Claim 7 is an independent claim that recites similar relevant features as those recited in claim 1. As described above with regard to the Examiner's rejection of claim 1 and claim 3, the teachings of Koh and Watanabe alone or in any allowable combination do not teach suggest, or describe the Appellant's invention with regard to claim 1 or claim 3. As such, and at least for the reason that neither Koh or Watanabe alone or in any combination teach suggest, or describe the Appellant's invention with regard to claim 1 and claim 3 for at least the reasons stated above, the Appellant respectfully submits that independent claim 7, which recites similar relevant features as claim 1, and dependent claims 8 and 9, which depend directly from independent claim 7, are also not rendered obvious by Koh in view of Watanabe.

More specifically, claim 7 specifically recites:

“A network for distributing a power signal in an optoelectronic circuit, said network comprising:

a plurality of separate electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths and wherein said pathways are joined only at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point;

means for coupling said power signal from a primary input to the common point of the first level;

terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal.”

The teachings of Koh and Watanabe alone or in any allowable combination do not teach suggest, or describe the Appellant's invention with regard to claim 7 and specifically for "a plurality of separate electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths" and "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal" for at least the reasons described above with respect to at least the Appellant's independent claim 1.

Therefore, the Appellant submits that claim 7 as it now stands, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

Furthermore, dependent claims 8 and 9 depend directly from claim 7 and recite additional features therefor. As such and for at least the reasons set forth herein, the Appellant submits that none of these claims are obvious with respect to the teachings of Koh and Watanabe, alone or in any allowable combination. Therefore the Appellant submits that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder. Reversal of the rejection is respectfully requested.

**III. THE EXAMINER ERRED IN REJECTING CLAIMS 1-5 AND 10-11 UNDER 35 U.S.C. § 103(a) BECAUSE THE CITED REFERENCE FAILS TO TEACH, SHOW, OR SUGGEST AT LEAST EACH OF THE SEGMENTS OF RESPECTIVE LEVELS HAVING EQUAL LENGTHS AND TERMINAL NODES COUPLED AT THE EXTREMITIES OF A LAST LEVEL FOR SUPPLYING A POWER SIGNAL TO A PLURALITY OF DEVICES SUCH THAT THE POWER SUPPLIED BY THE TERMINAL NODES TO EACH OF THE PLURALITY OF DEVICES IS SUBSTANTIALLY EQUAL.**

Claims 1-5 and 10-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe. The rejection is respectfully traversed.

The Examiner alleges that Watanabe discloses a network Fig. 12a for distributing a power signal in an optoelectronic circuit 350 comprising a plurality of

electrically conductive pathways forming at least one level, wherein the portions of the conductive pathways are interconnected; a plurality of segments 353a-353b forming each level, wherein each segment of the level is equal in length; means for coupling 347/352 the power signal from a primary input to a point at the center of a first level; terminal nodes 359a-b coupled at the extremities of a last level for supplying the power signal to devices that form at least a portion of the optoelectronic circuit 350; and wherein the number of segments connecting the primary input to each of the terminal nodes is equal.

The Examiner correctly concedes that Watanabe fails to teach that the network is used for supplying power signal to a plurality of devices. As such, the Examiner alleges that it would have been obvious to one of ordinary skill in the art at the time the invention was made to divide the device into multiple sections, since it is inherent that each portion of the single device of Watanabe would operate as an individual unit having its own power signal. The Examiner further alleges that it has been held that constructing a formerly integral structure in various elements involves only a routine skill in the art. The Appellant respectfully disagrees.

Watanabe teaches a surface electrode on the surface of an LED, wherein the surface electrode and the semiconductor layer are in electrical contact with each other at ends of the highest-order branches. (See Watanabe, ABSTRACT). In support of its invention Watanabe teaches:

**“At the ends of the sixth-order branches 358a and 358b, there are provided contact portions 359a and 359b for making ohmic contact with the underlying semiconductor layer 351.** Meanwhile, the rest of the surface electrode 347 other than the contact portions 359a and 359b is in a state in which a Schottky barrier are yielded on the surface of the semiconductor layer 351.” (See Watanabe, col. 16, lines 1-7). (emphasis added).

“Further, since the end portions of the sixth-order (highest-order) branches 358a and 358b and the semiconductor layer 351 are put into successful ohmic contact with each other through the contact portions 359a and 359b while the rest other than the end portions and the semiconductor layer 351 are brought into a state in which the current is suppressed from flowing by the Schottky barrier (i.e. a state in which current will not flow unless a certain high level of voltage is applied), the current can be injected only at the end portions of the surface electrode 351. Accordingly, the light easily goes out of the LED, which leads to further improved external quantum efficiency.” (See Watanabe, col. 16, lines 38-50).

The structure of the invention of Watanabe, as taught, includes contact portions in the highest-order branches for making ohmic contact with the underlying semiconductor layer. Watanabe fails though, to teach or suggest at least the invention of the Appellant's claim 1 as follows:

"A network for distributing a power signal in an optoelectronic circuit, said network comprising:

a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, **each of the segments of respective levels having equal lengths**, and wherein the segments of a next order higher level are formed at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point for the formation of the next order higher level;

means for coupling said power signal from a primary input to the common point of the first level; and

**terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit**, wherein the number of segments connecting said primary input to each of said terminal nodes is equal **such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal.**" (emphasis added).

In contrast to the invention of Watanabe, the Appellant's invention is directed at least in part to a power distribution network having very different structural limitations. In support of the present invention, the Appellant discloses:

"Terminal nodes are coupled to the endpoints of the last level of the H-tree. In this manner a conductive pathway is formed from the primary input to each terminal node, with portions of each conductive pathway being shared between two or more terminal nodes." (See Specification, page 7, lines 13-16).

"The first level is coupled to the primary input, at the center of the two horizontal segments of the H pattern. The conductive pathways distribute a power signal to terminal nodes 16 (represented by circles and as further indicated in the upper right hand quadrant for a portion of the terminal nodes of FIG. 3) on VLSI chip 20, wherein the distance from the primary input to each terminal node 16 is equal. In this illustrative example, **each terminal node 16 represents a VCSEL** and its associated driver." (See Specification, page 6, lines 22-29). (emphasis added).

"In operation of the present invention, the effect of voltage drops due to power supply line resistance are reduced when DC power is distributed to the terminal nodes of an optoelectronic circuit, namely the VCSELs in an array of

VCSELs of an OE-VLSI chip, with the H-tree power distribution network. Since the lengths of the conductive pathways to each terminal node are equal, there is greater uniformity of the voltage and current provided to each terminal node.” (See Specification, page 8, lines 3-8).

It is evident from the Appellant’s disclosure, that the Appellant’s invention is directed at least in part to a power distribution network for providing uniform power to external devices connected to each terminal node. As such, it is clear that the terminal nodes of the Appellant’s invention are not in ohmic contact with an underlying layer. Furthermore, in support of at least claim 1, the Appellant in the Specification specifically recites:

“Each ‘H’ pattern includes six equal length segments, with two segments in each of two parallel portions and two segments connected perpendicular at the midpoints of the parallel portions to form the H pattern.” (See Specification, page 7, lines 3-5).

The Appellant further recites:

“Since the length of each segment is equal for a respective level and the total number of segments to each terminal node is also equal, the length of the conductive pathway from the primary input to each terminal node is the same.” (See Specification, page 7, lines 16-19).

It is apparent from the sections of the disclosure presented above that the Appellant’s invention is directed at least in part to a power distribution network wherein each of the segments comprising each layer are of equal lengths and the total number of segments connecting each terminal node the primary input are equal. As such, the power provided to each of the plurality of terminal nodes at a last level and subsequently to each of a plurality of connected devices is substantially equal.

The invention of Watanabe is incapable of providing uniform power to devices connected to each terminal node because the surface electrode and the semiconductor layer are in electrical contact with each other at ends of the highest-order branches. The Appellant respectfully submits that at least the structural differences between the highest-order branches of the Appellant’s invention and the highest-order branches of the invention of Watanabe make the Appellant’s invention patentable over the invention

of Watanabe. The Appellant further submits that the structural configuration of the Appellant's highest-order branches are not obvious in view of the invention of Watanabe. The Appellant's invention and the invention of Watanabe are directed to two different devices having different structural limitations used for solving different problems. There is absolutely no teaching or suggestion in Watanabe for the Appellant's invention at least with respect to claim 1 and specifically for the structural limitations of the terminal nodes of the Appellant's invention as described above. More specifically, there is absolutely no teaching, suggestion or disclosure in Watanabe for "a plurality of electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths" (emphasis added), as taught by the Appellant's specification and claimed in at least the Appellant's claim 1.

Even further, there is absolutely no teaching, suggestion or disclosure in Watanabe for "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal" (emphasis added) as taught by the Appellant's specification and claimed in at least the Appellant's claim 1. Therefore, the Appellant respectfully submits that the Appellant's invention and the invention of Watanabe are directed to two different devices having different structural limitations used for solving different problems. There is absolutely no teaching or suggestion in Watanabe for the Appellant's invention at least with respect to claim 1 and specifically for the structural limitations of the Appellant's invention as described above.

As such, the Appellant respectfully submits that Watanabe does not teach or suggest the Appellant's claim 1. Specifically, the Appellant submits that the structural limitations of at least the Appellant's claim 1 are not taught or suggested by Watanabe. Therefore, the Appellant submits that independent claim 1, as it now stands, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

Likewise, independent claim 10 recites similar relevant features as recited in claim 1. As such, and for at least the reasons stated herein, the Appellant submits that

Watanabe does not teach or suggest independent claim 10, and that independent claim 10 as it now stands, also fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder. Even further, the Appellant respectfully submits, that even if the structural limitations of the Appellant's invention and the invention of Watanabe were the same (which the Appellant submits that they are not), the inventive method of claim 10 would not unpatentable because of the similarity of the structures.

Furthermore, dependent claims 2-5 and 11 depend directly from independent claims 1 and 10 and recite additional limitations therefore. As such and for at least the reasons set forth above, the Appellant submits that none of these claims are obvious with respect to the teachings of Watanabe. Therefore, the Appellant submits that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder. Reversal of the rejection is respectfully requested.

**IV. THE EXAMINER ERRED IN REJECTING CLAIMS 6-9 UNDER 35 U.S.C. § 103(a) BECAUSE THE CITED REFERENCE FAILS TO TEACH, SHOW, OR SUGGEST AT LEAST AT LEAST A PLURALITY OF ELECTRICALLY CONDUCTIVE PATHWAYS FORMING AT LEAST A FIRST LEVEL WHEREIN EACH LEVEL IS COMPRISED OF PLURALITY OF SEGMENTS LINEARLY EXTENDING FROM A COMMON POINT, EACH OF THE SEGMENTS OF RESPECTIVE LEVELS HAVING EQUAL LENGTHS, AND TERMINAL NODES COUPLED AT THE EXTREMITIES OF A LAST LEVEL FOR SUPPLYING A POWER SIGNAL TO A PLURALITY OF DEVICES SUCH THAT THE POWER SUPPLIED BY THE TERMINAL NODES TO EACH OF THE PLURALITY OF DEVICES IS SUBSTANTIALLY EQUAL WHEREIN THE TERMINAL NODES ARE VCSELS, WHEREIN EACH LEVEL IS AT LEAST ONE X-SHAPED PATTERN AND WHEREIN SAID CENTER OF SAID H-SHPED PATTERN IS THE MIDPOINT OF A THIRD BRANCH**

The Examiner rejected claims 6-9 under 35 U.S.C. § 103(a) as being unpatentable over Watanabe as applied to claims 1-5 and 10-11 above, and further in view of Olbright et al., (U.S. Patent 5,266,794, hereinafter "Olbright")/ Schneider et al.,

(U.S. Patent 5,351,256, hereinafter "Schneider") and Lebby et al., (U.S. Patent 5,337,397, hereinafter "Lebby"). The rejection is respectfully traversed.

Claim 6 depends directly from independent claim 1 and recites limitations thereof. The Examiner applied Watanabe to claim 6 as described above for the Examiner's rejection of claim 1. The Examiner alleges that Watanabe teaches all of the stated limitations except for the integrated circuits are VCSELs; instead Watanabe teach the integrated circuits are LEDs. The Appellant respectfully disagrees.

The Examiner correctly concedes that Watanabe does not teach that the integrated circuits are VCSELs as claimed in claim 6 of the Appellant's invention.

In addition and as described above, the teachings of Watanabe do not suggest or describe at least the Appellants' invention at least with regard to claim 1 for "a plurality of electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths" (emphasis added), or for "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal" (emphasis added).

Furthermore, the teachings of Olbright, Schneider, or Lebby, alone, do not teach, suggest, or describe the invention of the Appellant, at least with regard to claim 1. Neither Olbright, Schneider, nor Lebby, teach or suggest "a plurality of electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths" or "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal."

The Appellant further submits that there is no suggestion or motivation to combine the teachings of Watanabe and the teachings of Olbright, Schneider, or Lebby.

For prior art reference to be combined to render obvious a subsequent invention under 35 U.S.C. § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. Uniroyal v. Rudkin-Wiley, 5 U.S.P.SQ.2d 1434, 1438 (Fed. Cir. 1988). The teachings of the references can be combined only if there is some suggestion or incentive in the prior art to do so. In re Fine, 5 U.S.P.SQ.2d 1596, 1599 (Fed. Cir. 1988). Hindsight is strictly forbidden. It is impermissible to use the claims as a framework to pick and choose among individual references to recreate the claimed invention Id. at 1600; W.L. Gore Associates, Inc., v. Garlock, Inc., 220 U.S.P.Q. 303, 312 (Fed. Cir. 1983).

Moreover, the mere fact that a prior art structure could be modified to produce the claimed invention would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

The Appellant further submits that even if there was a motivation or suggestion to combine the references (which the Appellant believes that there is none), the teachings of Olbright, Schneider, and Lebby, either alone or in any allowable combination, fail to bridge the substantial gap between the Appellant's invention, and the teachings of Watanabe.

The Examiner further alleges that it is well known in the laser art that one may use either laser source (e.g. LED or VCSEL) as a matter of obvious design choice, see Olbright col. 8, lines 65-68/Schneider col. 1, lines 14-16/Lebby col. 3, lines 17-27. The Appellant respectfully disagrees.

The suggestion by the Examiner that the function of an LED is interchangeable with the function of a VCSEL in no way renders obvious a network for distributing a power signal wherein "a plurality of electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths"

and wherein “terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal” as claimed in at least the Appellant's claim

1. It is true that an LED may be interchangeable with a VCSEL in some applications when using said devices as lights sources, but the powering requirements or powering methods for an LED and a VCSEL are not similar at all. As stated above, the Appellant's invention is, at least in part, directed to powering a plurality of devices, such as VCSELs, that benefit in operation when receiving a uniform bias voltage among the plurality of devices. As such, to allege that one may use either a laser source (e.g. LED or VCSEL) as a matter of obvious design choice in this capacity (i.e. powering requirements) would be an incorrect statement or analogy.

As such, and at least for the reason that neither Olbright, Schneider, nor Lebby, alone or in any combination with Watanabe, teach suggest, or describe the Appellants' invention with regard to claim 1, the Appellants respectfully submit that dependent claim 6 is also not rendered obvious by Watanabe in view of Olbright, Schneider, or Lebby.

Therefore, the Appellant submits that claim 6 as it now stands, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

The Examiner further alleges that regarding claims 7-9, Watanabe teaches all the stated limitations except for the plurality of electrically conductive pathways being separate; instead, Watanabe teaches the pathways being formed of wider/broader pathways that diverge as it branches to a higher level/order. The Appellant respectfully disagrees.

Claim 7 is an independent claim that recites similar relevant features as those recited in claim 1. As described above with regard to the Examiner's rejection of claim 1, the teachings of Watanabe do not teach, suggest or describe at least the Appellants' invention with regard to claim 1 for “a plurality of electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths” or for “terminal nodes coupled at the extremities of a last level for

supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal". As independent claim 7 recites similar relevant features as those recited in claim 1, the Appellant respectfully submits that the teachings of Watanabe also do not teach, suggest or describe at least the Appellants' invention with regard to claim 7.

Furthermore, the teachings of Olbright, Schneider, or Lebby, alone, do not teach, suggest, or describe the invention of the Appellant, at least with regard to claim 1. Neither Olbright, Schneider, nor Lebby, teach or suggest "a plurality of electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths" or "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal."

The Appellant further submits that there is no suggestion or motivation to combine the teachings of Watanabe and the teachings of Olbright, Schneider, or Lebby. Even if there was a motivation or suggestion to combine (which the Appellant believes that there is none), the teachings of Olbright, Schneider, and Lebby, either alone or in any allowable combination, fail to bridge the substantial gap between the Appellant's invention, and the teachings of Watanabe.

Therefore, the Appellant submits that claim 7 as it now stands, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

Furthermore, dependent claims 8 and 9 depend directly from claim 7 and recite additional features therefor. As such and for at least the reasons set forth herein, the Appellant submits that none of these claims are obvious with respect to the teachings of Watanabe, Olbright, Schneider, and Lebby, alone or in any allowable combination. Therefore the Appellant submits that all these dependent claims also fully satisfy the

requirements of 35 U.S.C. § 103 and are patentable thereunder. Reversal of the rejection is respectfully requested.

### **Conclusion**

Thus, the Appellant submits that none of the claims presently in the application is anticipated under the provisions of 35 U.S.C. § 102(b) or obvious under the provisions of 35 U.S.C. § 103. Consequently, the Appellant believes all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue is earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring the issuance of an adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Jorge Tony Villabon, Esq. at (732) 53-9404 x 1131 or Mr. Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

For the reasons advanced above, Appellant respectfully urges that the rejections of claims 1-2, 4-5 and 10-11 as being unpatentable under 35 U.S.C. §102 and claims 1-11 as being obvious under 35 U.S.C. §103 are improper. Reversal of the rejections in this Appeal is respectfully requested.

Respectfully submitted,



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PENDING CLAIMS

1. (Previously Presented) A network for distributing a power signal in an optoelectronic circuit, said network comprising:

a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths, and wherein the segments of a next order higher level are formed at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point for the formation of the next order higher level;

means for coupling said power signal from a primary input to the common point of the first level; and

terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal.

2. (Previously Presented) The network of claim 1 wherein each level is at least one H-shaped pattern comprising first and second parallel branches each having a respective first and second midpoint, and a third branch interconnecting said first and second midpoints, and wherein said center of said H-shaped pattern is the midpoint of said third branch.

3. (Previously Presented) The network of claim 1 wherein each level is at least one X-shaped pattern comprising first and second branches each having a respective first and second midpoint and interconnecting said first and second branches at said midpoints, and wherein said center of said X-shaped pattern is the intersection of said first and second branches.

4. (Previously Presented) The network of claim 1 wherein said network is located on an optoelectronic chip.

5. (Previously Presented) The network of claim 1 wherein said terminal nodes are optoelectronic devices.

6. (Previously Presented) The network of claim 1 wherein said terminal nodes are VCSELS

7. (Previously Presented) A network for distributing a power signal in an optoelectronic circuit, said network comprising:

a plurality of separate electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths and wherein said pathways are joined only at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point;

means for coupling said power signal from a primary input to the common point of the first level;

terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal.

8. (Previously Presented) The network of claim 7 wherein each level is at least one H-shaped pattern comprising first and second parallel branches each having a respective first and second midpoint, and a third branch interconnecting said first and second midpoints, and wherein said center of said H-shaped pattern is the midpoint of said third branch.

9. (Previously Presented) The network of claim 7 wherein each level is at

least one X-shaped pattern comprising first and second branches each having a respective first and second midpoint and interconnecting said first and second branches at said midpoints, and wherein said center of said X-shaped pattern is the intersection of said first and second branches.

10. (Previously Presented) A method of distributing a power signal to a plurality of terminal nodes on an optoelectronic circuit, the method comprising the steps of:

receiving the power signal from a primary input; and

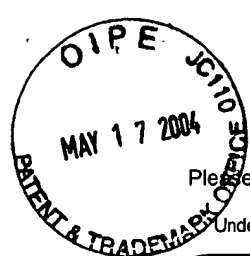
directing said power signal to said plurality of terminal nodes using an H-tree network, said H-tree network including at least a first level, wherein the first level is coupled to said primary input, and a last level includes said plurality of terminal nodes for supplying said power signal to a plurality of devices, each of said at least one level having a plurality of segments, each segment of a respective plurality is equal in length; and

wherein a number of segments from said primary input to each of said terminal nodes is equal such that the power supplied by each of the terminal nodes to each of the plurality of devices is substantially equal.

11. (Previously Presented) The method of claim 10, wherein the directing step further includes directing said power signal to said plurality of terminal nodes using an H-tree network,

wherein said plurality of segments are configured into at least one H pattern to form said at least first level; and

wherein said at least first level is configured into a hierarchical succession of H patterns.



05-18-04

PTO/SB/21 (08-03)

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Approved for use through 7/31/2006. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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**TRANSMITTAL  
FORM**

(to be used for all correspondence after initial filing)

Application Number	09/450,054
Filing Date	11/29/99
First Named Inventor	Krishnamoorthy
Group Art Unit	2828
Examiner Name	Cornelius H. Jackson
Attorney Docket Number	Krishnamoorthy 32

Total Number of Pages in This Submission

**ENCLOSURES (check all that apply)**

- |  |  |  |
|--|--|--|
| <input checked="" type="checkbox"/> Fee Transmittal Form<br><br><input type="checkbox"/> Fee Attached<br><br><input type="checkbox"/> Amendment / Response<br><br><input type="checkbox"/> After Final<br><br><input type="checkbox"/> Affidavits/declaration(s)<br><br><input type="checkbox"/> Extension of Time Request<br><br><input type="checkbox"/> Express Abandonment Request<br><br><input type="checkbox"/> Information Disclosure Statement<br><br><input type="checkbox"/> Certified Copy of Priority Document(s)<br><br><input type="checkbox"/> Response to Missing Parts/ Incomplete Application<br><br><input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53 | <input type="checkbox"/> Drawing(s)<br><br><input type="checkbox"/> Licensing-related Papers<br><br><input type="checkbox"/> Petition<br><br><input type="checkbox"/> Petition to Convert to a Provisional Application<br><br><input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address<br><br><input type="checkbox"/> Terminal Disclaimer<br><br><input type="checkbox"/> Request for Refund<br><br><input type="checkbox"/> CD, Number of CD(s) _____ | <input type="checkbox"/> After Allowance Communication to Group<br><br><input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences<br><input checked="" type="checkbox"/> Appeal Communication to Group ( <i>Appeal Notice, Brief, Reply Brief</i> )<br><br><input type="checkbox"/> Proprietary Information<br><br><input type="checkbox"/> Status Letter<br><br><input type="checkbox"/> Other Enclosure(s) (please identify below): |
| <b>Remarks</b>   |  |  |

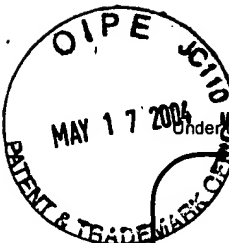
**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

Firm or Individual name	Eamon J. Wall, Reg. No. 39,414 Moser, Patterson & Sheridan, LLP
Signature	<i>EJ Wall</i>
Date	5/17/04

**CERTIFICATE Under 37 CFR 1.10**I hereby certify that this correspondence is being deposited on 5-17-04 with the United States Postal Service as Express Mail in an envelope addressed to: Commissioner for Patents, Mail Stop Appeal Brief – Patents, P.O. Box 1450, Alexandria, VA 22313-1450. Mailing Label No. EL967198976US

Typed or printed name	<i>C. W. Lson</i>		
Signature	<i>C. W. Lson</i>	Date	<u>5-17-04</u>

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon on the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



# FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) 330

## Complete if Known

Application Number	09/450,054
Filing Date	11/29/99
First Named Inventor	Krishnamoorthy
Examiner Name	Cornelius H. Jackson
Group / Art Unit	2828
Attorney Docket No.	Krishnamoorthy 32

## METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account

Deposit Account Number: 20-0782

Deposit Account Name: Moser, Patterson & Sheridan, LLP

The Director is authorized to: (Check all that apply)

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account

## FEE CALCULATION

1. BASIC FILING FEE					
Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	
SUBTOTAL (1)					(\$ 0)

## 2. EXTRA CLAIM FEES

Total Claims		** =	Extra Claims	X	Fee from below	=	Fee Paid
Independent Claims		** =	0	X		=	0
Multiple Dependent	0			X		=	0

Large Fee Code	Entity Fee (\$)	Small Fee Code	Entity Fee (\$)	Fee Description	
1202	18	2202	9	Claims in excess of 20	
1201	86	2201	43	Independent claims in excess of 3	
1203	290	2203	145	Multiple dependent claim, if not paid	
1204	86	2204	43	** Reissue independent claims over original patent	
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent	

SUBTOTAL (2) (\$ 0)

\*\*or number previously paid, if greater; For Reissues, see above

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330
1403	290	2403	145	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17 (q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) \_\_\_\_\_

\*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$ 330)

## SUBMITTED BY

## Complete (if applicable)

Name (Print/Type)	Eamon J. Wall	Registration No. Attorney/Agent	39,414	Telephone	(732)530-9404
Signature	EJ Wall			Date	5/17/04

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